AW-BT304W

BT5.0 SiP Module

Datasheet

Rev. 04

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(STD)

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Revision History

Revision	*Date*	*Description*	*Initials*	*Approved*
01	2018/05/10	Initial release	Licheng Wang	Chihhao Liao
02	2018/05/29	Update Pin Definition Update Pin Map to JEDEC specification Update Mechanical Information	Licheng Wang	Chihhao Liao
03	2020/01/09	Update BT spec	Licheng Wang	Chihhao Liao
04	2020/02/07	Modify 2.1.2 Pin number	Licheng Wang	Chihhao Liao

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AzureWave Technologies, Inc.

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1.0 Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the advanced **Bluetooth** SiP module - **AW-BT304W.**

AW-BT304W is the optimal solution for applications in wireless input, wearables, and Internet of Things (IoT) devices. Also is a member of the WICED Core ELP, a highly integrated wireless MCU family. It is an enhanced ultra-low power (ULP), multi-protocol, highly integrated wireless MCU, that provides the best-in-class combination of ULP, performance and integration. Combined with the WICED-PRO SDK, the **AW-BT304W** enables a complete audio ecosystem, helping audio accessory vendors to deploy value added and differentiated products, also is a BT 5.0 compliant SOC with support for Bluetooth BR, BLE, 2 Mbps LE, and low power consumption EDR limited to 0 dBm.

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1.2 Features

1.2.1 Bluetooth

■ Complies with Bluetooth Core Specification version 5.0 including Basic Rate (BR) BR/BLE
■ Supports Cypress proprietary LE data rate up to 2Mbps
■ BLE HID profile version 1.00 compliant
■ Bluetooth Device ID profile version 1.3 compliant
■ Supports Generic Access Profile (GAP)
■ Supports Adaptive Frequency Hopping (AFH)
■ Excellent receiver sensitivity
■ Programmable output power control
■ Integrated ARM Cortex-M4 microprocessor core floating point unit (FPU)
■ On-chip power-on reset (POR)
■ Support for EEPROM and serial flash interfaces
■ Integrated buck and low dropout (LDO) regulator
■ On-chip software controlled PMU
■ Programmable key scan matrix interface, up to 8 × 20 key-scanning matrix
■ Auxiliary ADC with up to 28 analog channels
■ On-chip support for serial peripheral interface (SPI) (master and slave modes)
■ Cypress Serial Communications (BSC) interface (compatible with NXP I2C slaves)
■ Support for LEAII (LE packets up to 255 bytes)
■ Support for 1.2V button-cell battery operations (2032,2025, 13, 312, and 675 types)
■ Drift tracking and Automatic Radio Sequencer (ARS)
■ RoHS compliant
■ Support Wireless Audio Stereo Sync (WASS) Function

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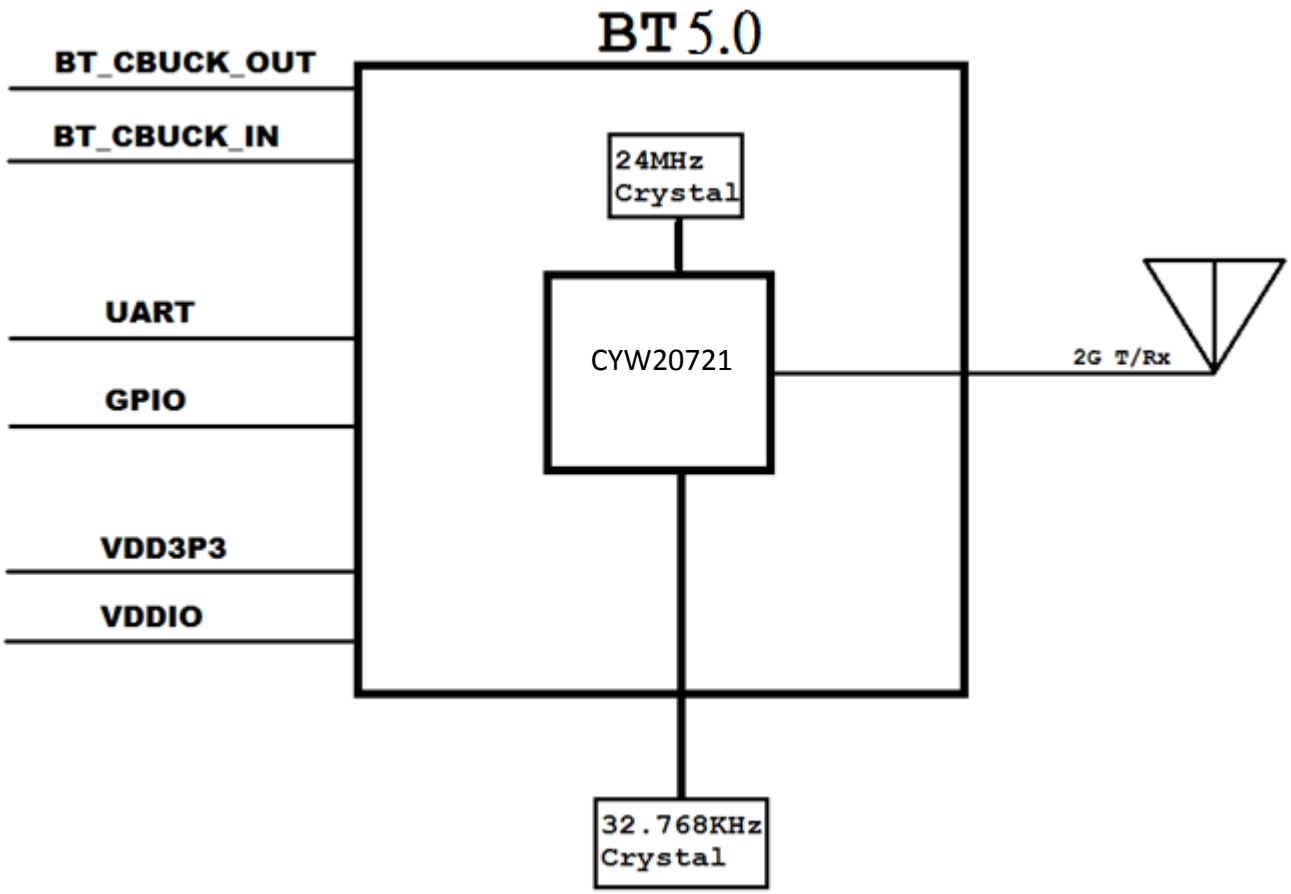
1.3 Block Diagram

A simplified block diagram of the AW-BT304W module is depicted in the figure below.



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1.4 Specifications Table

1.4.1 General

Features	Description
Product Description	Bluetooth 5.0 SiP Module
Major Chipset	CYW20721
Host Interface	Bluetooth : UART
Dimension	6.0mm x 5.2mm x 0.9mm (typ)
Package	SiP
Weight	0.075g
MSL Level	LV3
RF Shielding	EMI Coating

1.4.2 Bluetooth

Features	Description
Bluetooth Standard	BT5.0+Enhanced Data Rate (EDR)+BLE
Bluetooth VID/PID	TBD
Frequency Rage	2402~2480MHz
Modulation	GFSK (1Mbps), Π/4 DQPSK (2Mbps) and 8DPSK (3Mbps)
Output Power (Typical)	■ BR: 4 dBm +/- 2 dBm (TBC) ■ EDR: 0 dBm +/- 2 dBm (TBC) ■ Low Energy: 4 dBm +/- 2 dBm (TBC)
Receiver Sensitivity (Typical)	■ BR: -88 dBm (BER<0.1%) (TBC) ■ EDR(2M): -91 dBm (BER<0.1%) (TBC) ■ EDR(3M): -83 dBm (BER<0.1%) (TBC) ■ Low Energy: -91 dBm (BER<0.1%) (TBC)

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1.4.3 Operating Conditions

Features	Description
Operating Conditions	
Voltage	Input supply voltage DC,VBAT: 1.9V~3.63V Typ:3.3V Input supply voltage VDDIO: 1.62V~3.63V Typ:1.8V
Operating Temperature	-30~85 ℃
Operating Humidity	<85%
Storage Temperature	-40~125 ℃
Storage Humidity	< 60 %
ESD Protection	
Human Body Model	2 KV
Changed Device Model	500 V

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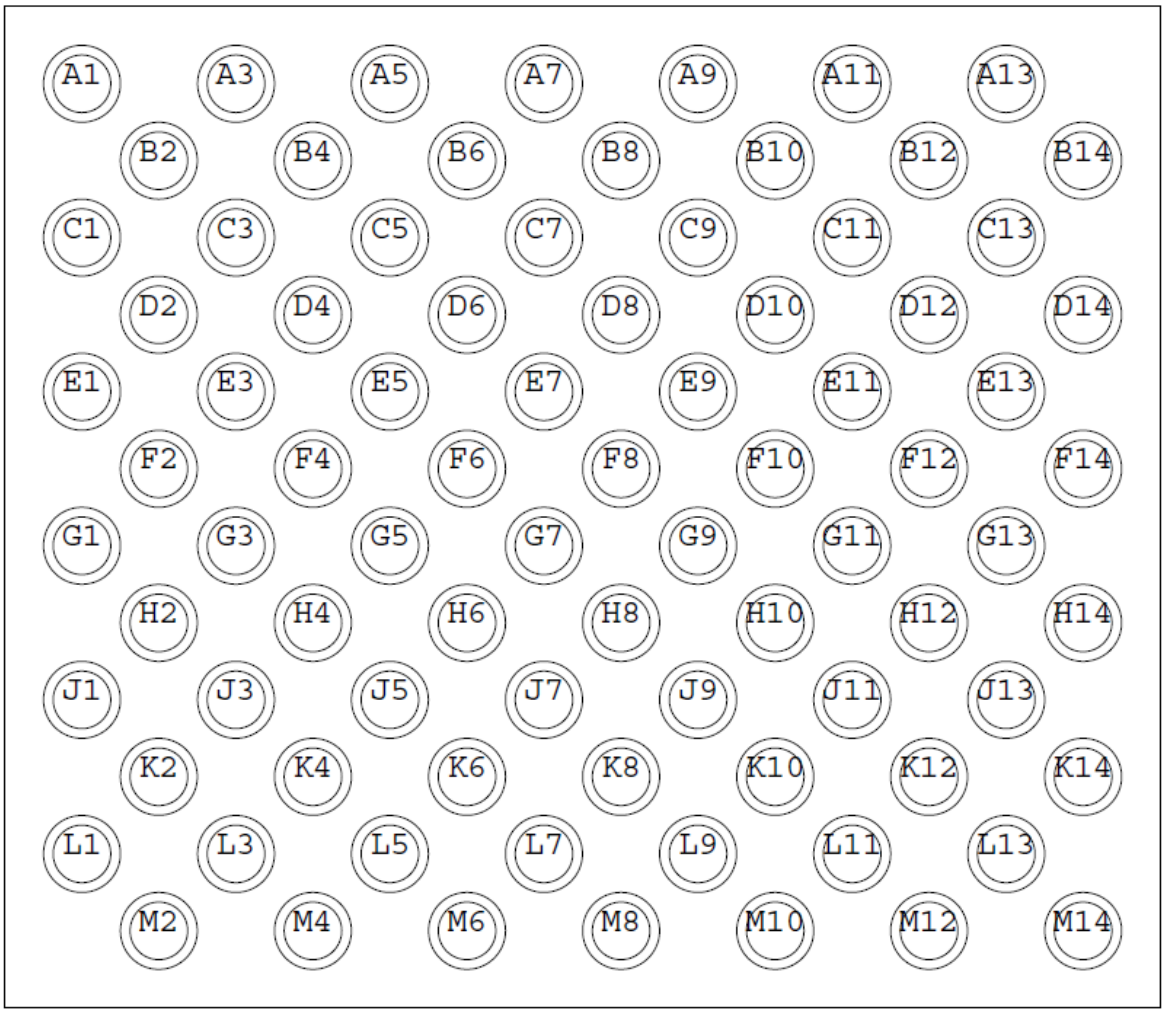
2.0 Pin Definition

AW-BT304W Top View PCB Layout Footprint



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2.1 Pin Map

Pin No.	Definition	Basic Description	Type	Voltage
A1	GND	Connect to GND	GND	
A3	GND	Connect to GND	GND	
A5	GND	Connect to GND	GND	
A7	GND	Connect to GND	GND	
A9	GND	Connect to GND	GND	
A11	RF	BT RF TX/RX path	RF	
A13	GND	Connect to GND	GND	
B2	VDD3P3	Core Buck Input	VCC	3.3V
B4	BT_CBUCK_IN	Internal Buck voltage generation pin	VCC	
B6	GND	Connect to GND	GND	
B8	P37	■ GPIO: P37 ■ A/D converter input 2 ■ Supermux I/O functions as defined in Table 1	I/O	
B10	GND	Connect to GND	GND	
B12	GND	Connect to GND	GND	
B14	GND	Connect to GND	GND	
C1	BT_CBUCK_OUT	Internal Buck voltage generation pin	VCC	3.3V
C3	GND	Connect to GND	GND	
C5	P27	■ GPIO: P27 ■ Current: 16 mA sink ■ Supermux I/O functions as defined in Table 1	I/O	
C7	P29	■ GPIO: P29 ■ Optical control output: QOC3 ■ A/D converter input 10 ■ Current: 16 mA sink	I/O	

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		■ Supermux I/O functions as defined in Table 1		
C9	P33	■ GPIO: P33 ■ A/D converter input 6 ■ Supermux I/O functions as defined in Table 1	I/O	
C11	GND	Connect to GND	GND	
C13	GND	Connect to GND	GND	
D2	P32	■ GPIO: P32 ■ A/D converter input 7 ■ Supermux I/O functions as defined in Table 1	I/O	
D4	P30	■ GPIO: P30 ■ A/D converter input 9 ■ Supermux I/O functions as defined in Table 1	I/O	
D6	P25	■ GPIO: P25 ■ Supermux I/O functions as defined in Table 1	I/O	
D8	P13	■ GPIO: P13 ■ A/D converter input 22 ■ Supermux I/O functions as defined in Table 1	I/O	
D10	P38	■ GPIO: P38 ■ A/D converter input 1 ■ Supermux I/O functions as defined in Table 1	I/O	
D12	P4	■ GPIO: P4 ■ Keyboard scan input (row): KSI4 ■ Supermux I/O functions as defined in Table 1	I/O	
D14	GND	Connect to GND	GND	
E1	P31	■ GPIO: P31 ■ A/D converter input 8	I/O	

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		■ Supermux I/O functions as defined in Table 1		
E3	NC			
E5	P0	■ GPIO: P0 ■ Keyboard scan input (row): KSI0 ■ A/D converter input 29 ■ Supermux I/O functions as defined in Table 1.	I/O	
E7	P18	■ GPIO: P18 ■ A/D converter input 17 ■ Supermux I/O functions as defined in Table 1	I/O	
E9	P34	■ GPIO: P34 ■ A/D converter input 5 ■ Supermux I/O functions as defined in Table 1	I/O	
E11	P7	■ GPIO: P7 ■ Keyboard scan input (row): KSI7 ■ Supermux I/O functions as defined in Table 1	I/O	
E13	P6	■ GPIO: P6 ■ Keyboard scan input (row): KSI6 ■ Supermux I/O functions as defined in Table 1	I/O	
F2	P24	■ GPIO: P24 ■ Supermux I/O functions as defined in Table 1	I/O	
F4	P35	■ GPIO: P35 ■ A/D converter input 4 ■ Supermux I/O functions as defined in Table 1	I/O	
F6	P23	■ GPIO: P23 ■ A/D converter input 12 ■ Supermux I/O functions as defined in Table 1	I/O	

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F8	P16	■ GPIO: P16 ■ A/D converter input 19 ■ Supermux I/O functions as defined in Table 1	I/O	
F10	P17	■ GPIO: P17 ■ A/D converter input 18 ■ Supermux I/O functions as defined in Table 1	I/O	
F12	P5	■ GPIO: P5 ■ Keyboard scan input (row): KSI5 ■ Supermux I/O functions as defined in Table 1	I/O	
F14	BT_GPIO4	General Purpose I/O: Can also be configured as a GCI Pin	I/O	
G1	BT_XTAL_32K_I	Low-power oscillator input.	I	
G3	P26	■ GPIO: P26 ■ Current: 16 mA sink ■ Supermux I/O functions as defined in Table 1	I/O	
G5	P12	■ GPIO: P12 ■ A/D converter input 23 ■ Supermux I/O functions as defined in Table 1	I/O	
G7	P11	■ GPIO: P11 ■ A/D converter input 24 ■ Supermux I/O functions as defined in Table 1	I/O	
G9	P8	■ GPIO: P8 ■ A/D converter input 27 ■ Supermux I/O functions as defined in Table 1	I/O	
G11	GND	Connect to GND	I/O	
G13	BT_GPIO5	General Purpose I/O: Can also be configured as a GCI Pin	I/O	

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H2	P36	■ GPIO: P36 ■ A/D converter input 3 ■ Supermux I/O functions as defined in Table 1	I/O	
H4	P1	■ GPIO: P1 ■ Keyboard scan input (row): KSI1 ■ A/D converter input 28 ■ Supermux I/O functions as defined in Table 1	I/O	
H6	NC			
H8	GND	Connect to GND	GND	
H10	GND	Connect to GND	GND	
H12	BT_HOST_WAKE	A signal from the AW-BT304W device to the host indicating that the Bluetooth device requires attention.	O	
H14	BT_DEV_WAKE	A signal from the host to the AW-BT304W indicating that the host requires attention.	I	
J1	BT_XTAL_32K_O	Low-power oscillator output	O	
J3	P10	■ GPIO: P10 ■ Keyboard scan output (column): KSO2 ■ A/D converter input 25 ■ Supermux I/O functions as defined in Table 1	I/O	
J5	P3	■ GPIO: P3 ■ Keyboard scan input (row): KSI3 ■ Supermux I/O functions as defined in Table 1	I/O	
J7	P9	■ GPIO: P9 ■ A/D converter input 26 ■ External T/R switch control: tx_pd ■ Supermux I/O functions as defined in Table 1	I/O	

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J9	GND	Connect to GND	GND	
J11	BT_GPIO2	General Purpose I/O: Can also be configured as a GCI	I/O	
		Pin		
J13	BT_GPIO3	General Purpose I/O: Can also be configured as a GCI Pin	I/O	
K2	P21	■ GPIO: P21 ■ A/D converter input 14 ■ Supermux I/O functions as defined in Table 1	I/O	
K4	P28	■ GPIO: P28 ■ A/D converter input 11 ■ Current: 16 mA sink ■ Supermux I/O functions as defined in Table 1	I/O	
K6	P2	■ GPIO: P2 ■ Keyboard scan input (row): KSI2 ■ Supermux I/O functions as defined in Table 1	I/O	
K8	GND	Connect to GND	GND	
K10	BT_UART_TXD	UART serial input. Serial data input for	O	
		the HCI UART interface.		
K12	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.	I	
K14	RST_N[1]	Active-low system reset with open-drain output and internal pull-up resistor.	I	1.8V
L1	GND	Connect to GND	GND	
L3	P14	■ GPIO: P14	I/O	

[1] The RST_N pinout support Reset Delay Time,

Release Delay Time(typ)	Release Delay Time(min~max)
45.6ms	36.45~54.6(ms)

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		■ A/D converter input 21 ■ Supermux I/O functions as defined in Table 1		
L5	GND	Connect to GND	GND	
L7	GND	Connect to GND	GND	
L9	BT_UART_CTS_N	Clear to send (CTS) for HCI UART interface. Leave unconnected if not used.	I/O	
L11	BT_UART_RTS_N	Request to send (RTS) for HCI UART interface. Leave unconnected if not used.	I	
L13	GND	Connect to GND	GND	
M2	P22	■ GPIO: P22 ■ A/D converter input 13 ■ Supermux I/O functions as defined in Table 1	I/O	
M4	NC			
M6	GND	Connect to GND	GND	
M8	GND	Connect to GND	GND	
M10	P15	■ GPIO: P15 ■ A/D converter input 20 ■ Supermux I/O functions as defined in Table 1	I/O	
M12	VDDIO	VDDIO supply for BT I/O	VCC	
M14	GND	Connect to GND	GND	

a. All GPIOs are super mux. All GPIOs can be programmed for any alternative functions as listed in 2.1.1 Table 1 and Table 2.
b. During power-on reset, all inputs are disabled.
c. P15 and P37 should not be driven high externally while the part is held in reset (they can be floating or driven low). Failure to do so may cause some current to flow through these pins until the part comes out of reset.

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2.1.1. GPIO Supermux Input/Output Function List

Input	Description
SWDCK	Serial Wire Debugger Clock
SWDIO	Serial Wire Debugger I/O
spiffy1_clk[s]	SPIFFY 1 Clock (Slave)
spiffy1_cs[s]	SPIFFY 1 Chip Select (Slave)
spiffy1_mosi[s]	SPIFFY 1 MOSI (Slave)
spiffy1_miso[m]	SPIFFY 1 MISO (Master)
spiffy1_io2	SPIFFY 1 I/O 2 (Quad SPI)
spiffy1_io3	SPIFFY 1 I/O 3 (Quad SPI)
spiffy1_int[s]	SPIFFY 1 Interrupt (Slave)
spiffy2_clk[s]	SPIFFY 2 Clock (Slave)
spiffy2_cs[s]	SPIFFY 2 Chip Select (Slave)
spiffy2_mosi[s]	SPIFFY 2 MOSI (Slave)
spiffy2_miso[m]	SPIFFY 2 MISO (Master)
spiffy2_io2	SPIFFY 2 I/O 2
spiffy2_io3	SPIFFY 2 I/O 3

Input	Description
spiffy2_int[s]	SPIFFY 2 Interrupt (Slave)
puart_rx	Peripheral UART RX
puart_cts_n	Peripheral UART CTS
SCL	I2C Clock
SDA	I2C Data
SCL2	I2C2 Clock
SDA2	I2C2 Data
PCM_IN	PCM Input
PCM_CLK	PCM Clock
PCM_SYNC	PCM Sync
I2S_DI	I2S Data Input
I2S_WS	I2S Word Select
I2S_CLK	I2S Clock
PDM_IN_Ch_1	PDM Input Channel 1
PDM_IN_Ch 2	PDM Input Channel 2

Table1 GPIO Supermux Input Functions

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Output	Description
do_P# (data out of GPIO. For example: 0)	
kso0	Key Scan output 0
kso1	Key Scan output 1
kso2	Key Scan output 2
kso3	Key Scan output 3
kso4	Key Scan output 4
kso5	Key Scan output 5
kso6	Key Scan output 6
kso7	Key Scan output 7
kso8	Key Scan output 8
kso9	Key Scan output 9
kso10	Key Scan output 10
kso11	Key Scan output 11
kso12	Key Scan output 12
kso13	Key Scan output 13
kso14	Key Scan output 14
kso15	Key Scan output 15

Output	Description
kso16	Key Scan output 16
kso17	Key Scan output 17
kso18	Key Scan output 18
kso19	Key Scan output 19
do_P# ^ pwm0	PWM Channel 0
do_P# ^ pwm1	PWM Channel 1
do_P# ^ pwm2	PWM Channel 2
do_P# ^ pwm3	PWM Channel 3
do_P# ^ pwm4	PWM Channel 4
do_P# ^ pwm5	PWM Channel 5
aclk0	Auxiliary clock Output 0
aclk1	Auxiliary clock Output 1
HID_OFF	HID-OFF Indicator
pa_ramp	External PA ramp
tx_pd	External PA Control Signal

Output	Description
~tx_pd	External PA Control Signal
SWDIO	Serial Wire Debugger Input/ Output
SDA2	I2C 2 Data
SCL2	I2C 2 Clock
puart_tx (uart2_tx)	Peripheral UART TX
puart_rts_n (uart2_rts_n)	Peripheral UART RTS
spiffy1_CLK	SPIFFY 1 Clock
spiffy1_CS	SPIFFY 1 Chip Select
spiffy1_MOSI	SPIFFY 1 MOSI
spiffy1_MISO	SPIFFY 1 MISO
spiffy1_IO2	SPIFFY I/O 2
spiffy1_IO3	SPIFFY I/O 3
spiffy1_INT	SPIFFY Interrupt
spiffy1_DCX	MIPI-DBI Data/Command Indicator
spiffy2_CLK	SPIFFY 2 Clock
spiffy2_CS	SPIFFY 2 Chip Select
spiffy2_MOSI	SPIFFY 2 MOSI

Output	Description
spiffy2_MISO	SPIFFY 2 MISO
spiffy2_IO2	SPIFFY 2 I/O 2
spiffy2_IO3	SPIFFY 2 I/O 3
spiffy2_INT	SPIFFY 2 Interrupt
spiffy2_DCX	MIPI-DBI Data/Command Indicator
pcm_in_o	PCM IN
pcm_out_o	PCM Out
pcm_bclk_o	PCM Bit Clock
pcm_sync_o	PCM Sync Output
i2s_ssd	I2S Slave Serial Data
i2s_sws	I2S Slave Word Select
i2s_sck	I2S Slave Clock
i2s_msd	I2S Master Serial Data
i2s_mws	I2S Master Word Select
i2s_mck	I2S Master Clock

Table 2 GPIO Supermux Output Functions

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2.1.2. Reference for how to connect to Cirrus logic codec[2]

Pin Available for I2C		
Pin No.	Definition	I2C function
F8	P16	I2C_SDA
F10	P17	I2C_SCL

Pin Available for SPIO-FLASH:		
Pin No.	Definition	I2C function
E5	P0	SPI_MOSI
H4	P1	SPI_MISO
J5	P3	SPI_CLK
D2	P32	SPI_CS

Pin Availble for I2S		
Pin No.	Definition	I2C function
G9	P8	I2S_DO
J7	P9	I2S_DI
G7	P11	I2S_BCLK
G5	P12	I2S_LRCLK

Pin Available for SPI1-CODEC		
Pin No.	Definition	I2C function
F4	P35	SPI_MOSI
H2	P36	SPI_MISO
D4	P30	SPI_CLK
E11	P7	SPI_CS

Table 3 GPIO Supermux for reference to connect CODEC

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[2] Table 3 is only for reference, please confirm it with CODEC vendor.

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3.0 Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD3P3	VBAT input	1.9	3.3	3.63	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDDIO	I/O voltage	1.62	1.8	3.63	V

3.3 Digital IO Pin DC Characteristics

VDDIO=3 V

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	2.4	-	-	V
V_{IL}	Input low voltage	--	-	0.8	V
V_{OH}	Output high voltage	2.55	-	-	V
V_{OL}	Output low voltage	-	-	0.5	V

VDDIO=1.8 V

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	1.4	-	-	V
V_{IL}	Input low voltage	--	-	0.4	V
V_{OH}	Output high voltage	1.35	-	-	V
V_{OL}	Output low voltage	-	-	0.5	V

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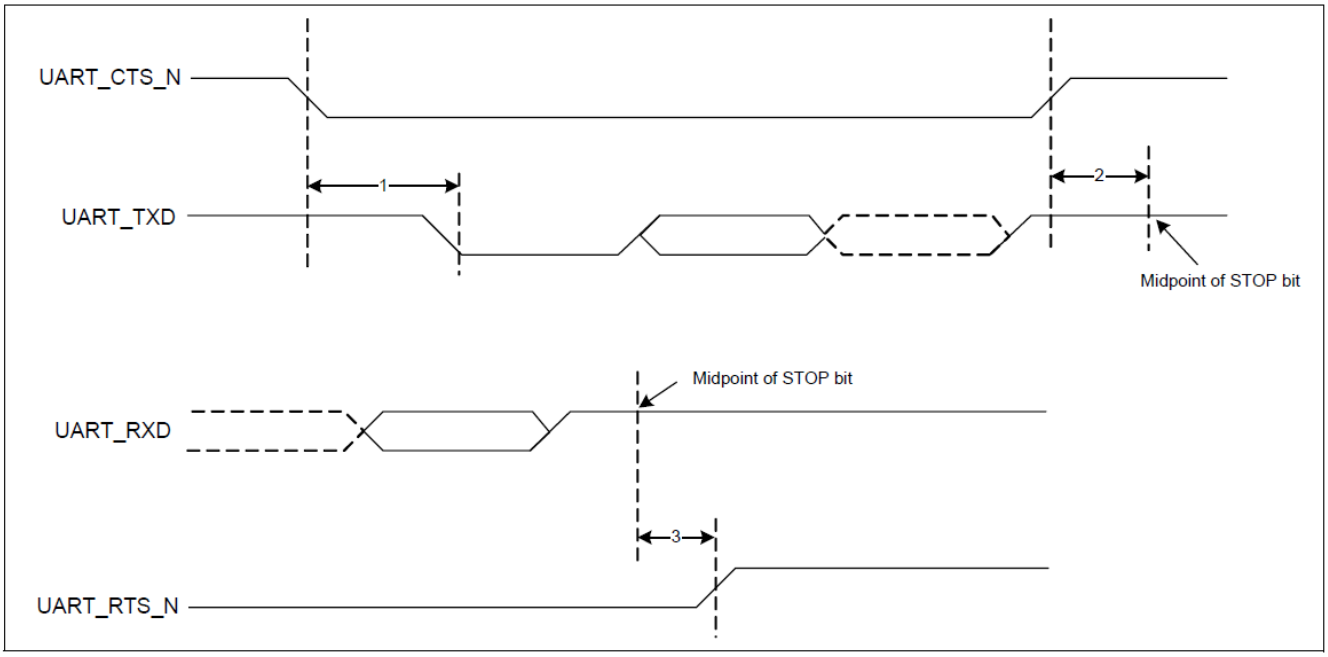
3.4 Timing

3.4.1 UART Timing

UART Timing Specifications

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid.	–	–	1.50	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit.	–	–	0.67	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high.	–	–	1.33	Bit periods

UART Timing



3.4.2 SPI Timing

SPI Mode 0 and 2

Reference	Characteristics	Min.	Max.	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns

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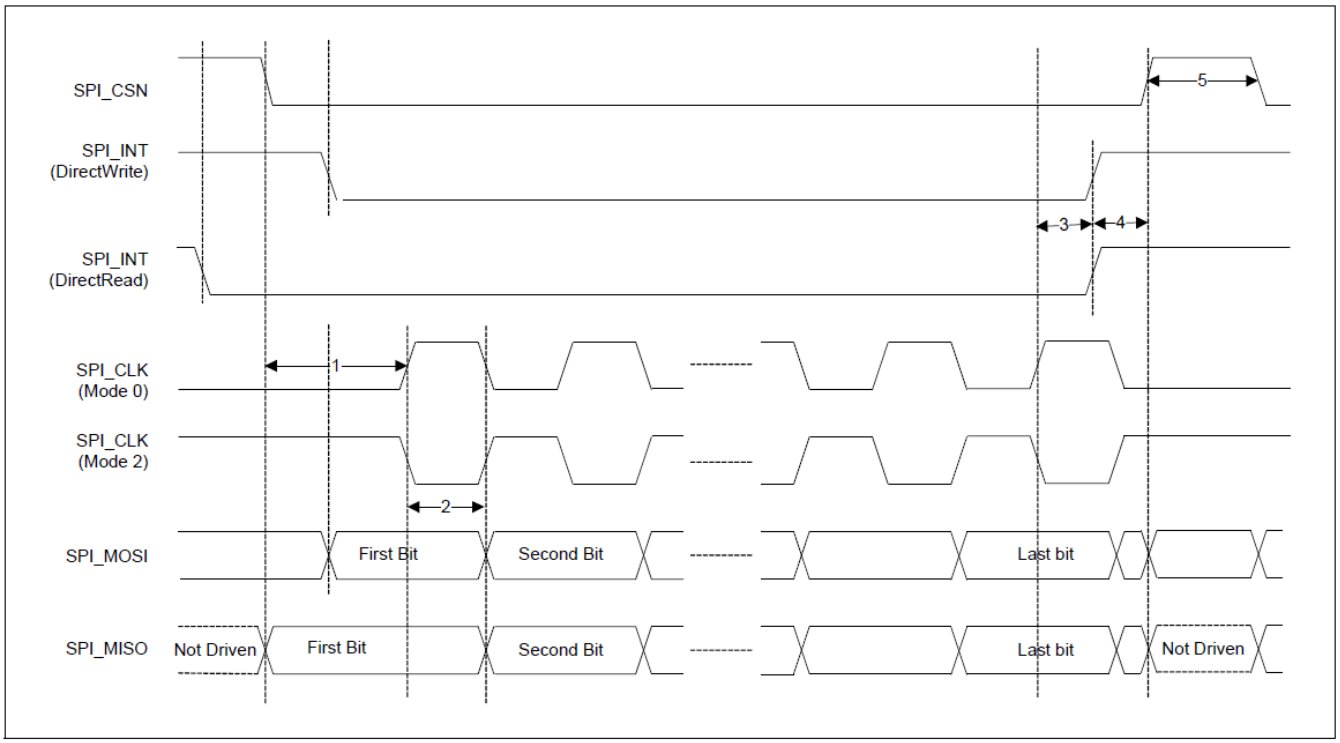
SPI Timing, Mode 0 and 2



3.5 Power Consumption

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BLUETOOTH

No.	Mode	Packet Type	RF Power (dBm)	VBAT=3.0V	
				Max.	Avg.
1	Sleep	n/a	n/a	53.4uA	49.4uA
2	Transmit	DH5	2.13	6.8mA	6.6mA
3	Receive	3DH5	n/a	6.3mA	6.2mA
4	LE Transmit	n/a	2	6.0mA	5.7mA
5	LE Receive	n/a	n/a	6.5mA	6.3mA

*Current Unit: mA

Note:1.The power consumption data were measured when NB operated in DC (battery) mode
2. Wifi function is disabled.

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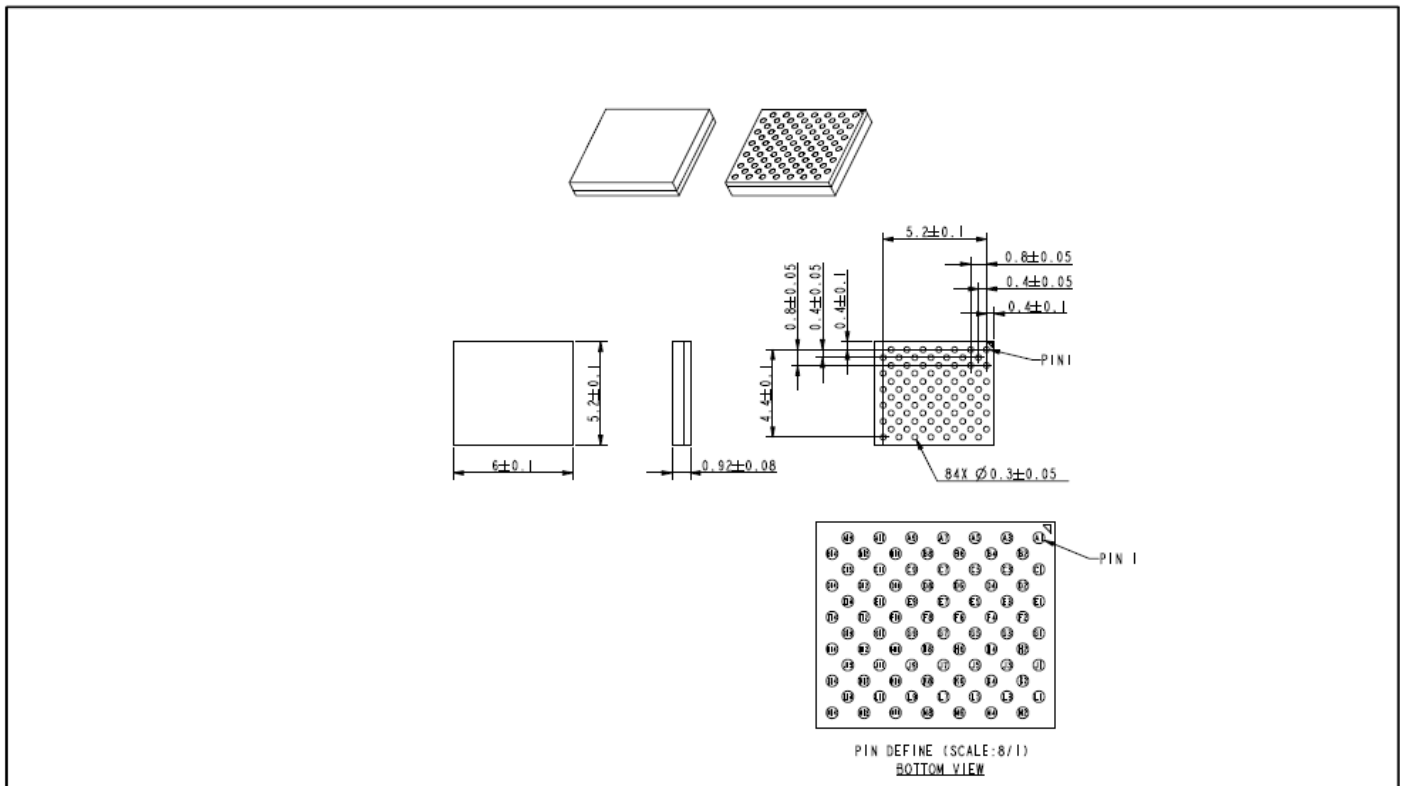
4.0 Mechanical Information

4.1 Mechanical Drawing



			AzureWave					MODEL NO.		DESCRIPTION					DOCUMENT LEVEL	APPROVAL
								1304W		MECHANICAL OUTLINE DRAWING (NON-SOLDER)					CONFIDENTIAL	
			DIM.	0~80	80~180	180~315	315~800	PART NO.	DRAWING NO.	MATERIAL	UNIT	SCALE	REV	PAGE	DATE	DESIGNED
ITEM	DESCRIPTION	DATE	TOL.	±0.1	±0.15	±0.20	±0.25		1304W-COD-001		mm	4/1	A	1/1	2018/05/29	STEVE CHANG

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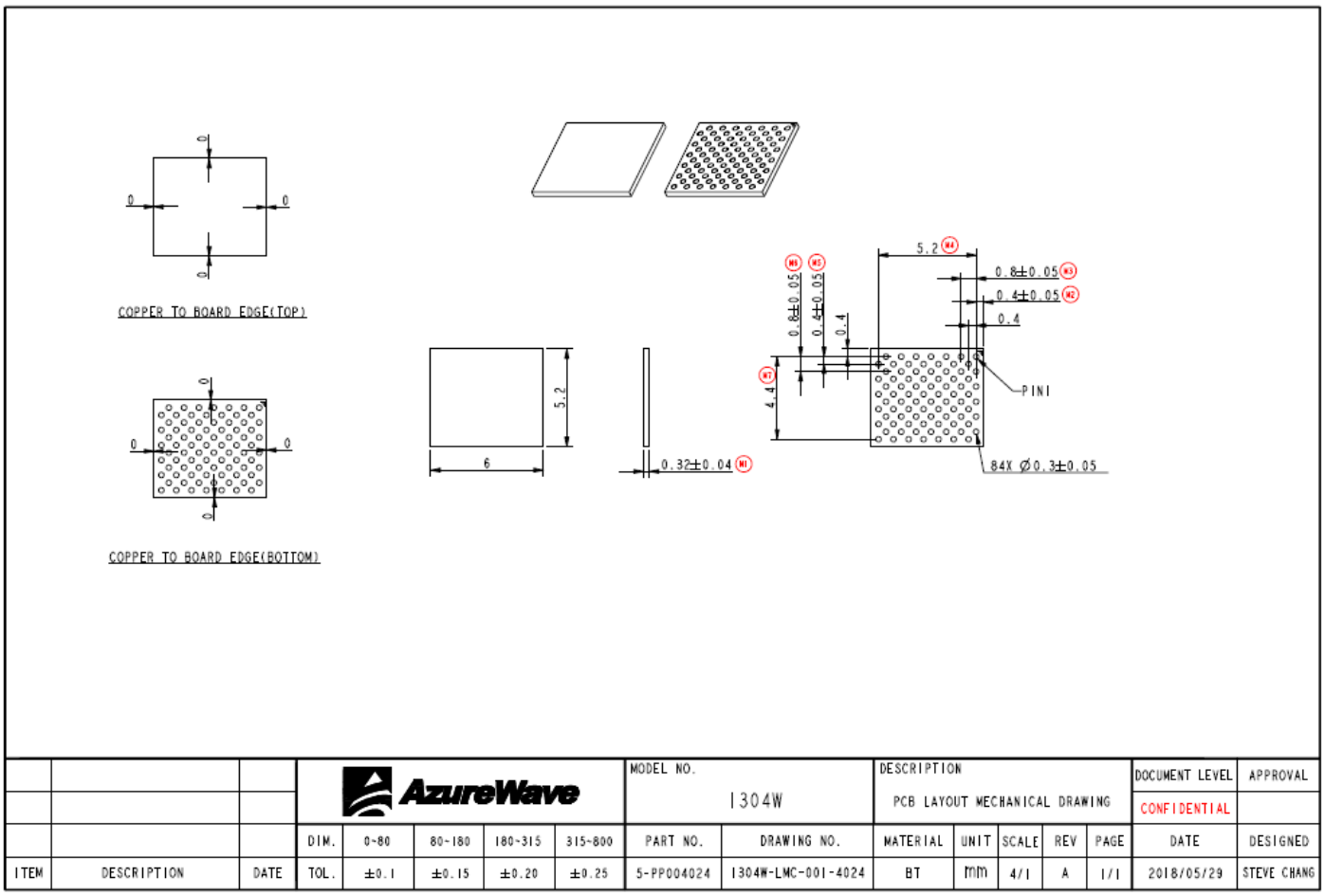
4.2 PCB Footprint



			AzureWave					MODEL NO.		DESCRIPTION					DOCUMENT LEVEL	APPROVAL
								1304W		PCB LAYOUT MECHANICAL DRAWING					CONFIDENTIAL	
			DIM.	0~80	80~180	180~315	315~800	PART NO.	DRAWING NO.	MATERIAL	UNIT	SCALE	REV	PAGE	DATE	DESIGNED
ITEM	DESCRIPTION	DATE	TOL.	±0.1	±0.15	±0.20	±0.25	5-PP004024	1304W-LMC-001-4024	BT	mm	4/1	A	1/1	2018/05/29	STEVE CHANG

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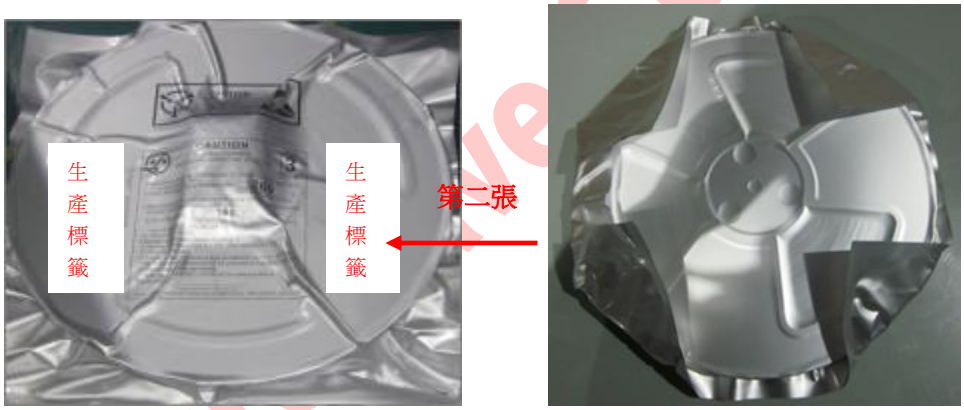
5. Packaging Information

5-1 在卷帶無孔的輪盤中間放置乾燥劑，圖示位置放置濕度指示卡及貼上生產標籤

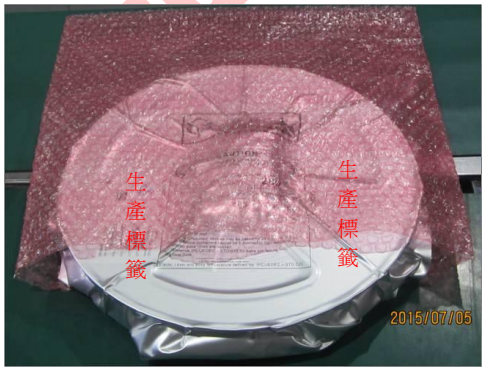
整盤產品的包裝數量為 3500PCS.

5-2 真空後的產品，在輪盤中間粘貼生產標籤，鋁箔袋 4 角向後折起

備註：合批產品，在下圖所示位置粘貼第二張生產標籤，不可覆蓋警語標籤和 ESD 標籤



5-3 將包裝好的鋁箔袋裝入氣泡袋中，ESD 及警告標語標籤朝向鋁箔袋封口方向，如下圖所示



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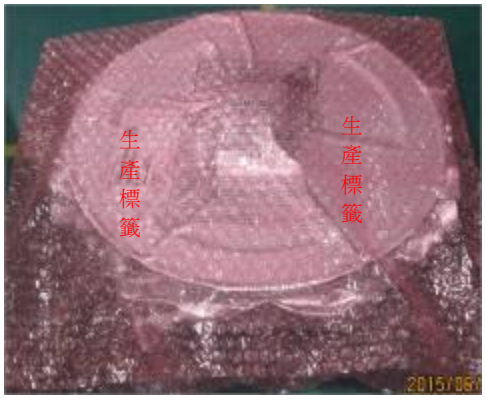
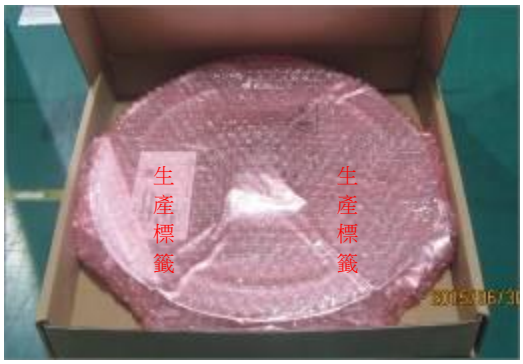
5-4 放置好的產品如下圖所示



5-5 將氣泡袋開口處多餘的材料向後折起，平整放入內箱中，如下圖所示



5-6 在內箱上蓋左下角位置粘貼生產標籤

備註：如有合批產品，在下圖所示位置粘貼第二張生產標籤

5-7 合上內盒盒蓋，在開口處封上一層透明膠帶，如下圖所示

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5-8 在外箱中依次放入 5pcs 內箱，內箱開口端向下,擺放位置如下圖所示

5-9 在外箱正面依1,2,3,4,5順序粘貼生產標籤,外箱粘貼的生產標籤需與此包裝中內箱上的生產標籤保持一致，若內箱上生產標籤有兩張的，並排粘貼於外箱對應生產標籤旁邊，如下圖所示

5-10 用帶有海華 logo 的膠帶密封包裝，封成“工”字形；出貨標籤貼於外箱正面左上角，如下圖所示

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